In the Claims

1-16 (Canceled)

17. (Previously Presented) A memory cell, comprising:

a transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region, that are vertically aligned;

a trench capacitor having a second plate of polycrystalline material formed in a trench and a first plate coupled to the second source/drain region without an intervening conductor, the first plate having an etch-roughened surface, the second plate surrounding at least a portion of the first plate; and

an insulator layer that separates the second plate from the etch-roughened surface of the first plate, wherein the transistor further includes a gate adjacent to the body region and the gate being directly above the second plate.

18. (Previously Presented) The memory cell of claim 17, wherein the second polycrystalline semiconductor plate comprises polysilicon.

19. (Previously Presented) The memory cell of claim 17, wherein the first plate comprises a heavily doped n-type silicon substrate.

20.-25. (Canceled)

26. (Previously Presented) A memory device, comprising:

an array of memory cells, each of the memory cells including a vertical access transistor that is coupled to a trench capacitor, wherein a first plate of the trench capacitor is coupled to a second source/drain region of the vertical access transistor without an intervening conductor, the first plate including a micro-roughened surface layer of porous polysilicon, wherein the trench capacitor includes a second plate disposed adjacent to the first plate and surrounding the first

plate, and wherein the vertical access transistor includes a body region vertically aligned with the second source/drain region, and a gate adjacent to the body region, the gate being directly above the second plate;

a number of bit lines, each of the bit lines being selectively coupled to a number of the memory cells at a first source/drain region of the vertical access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to the gate of the vertical access transistor of each memory cell of the number of the memory cells; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines for selectively accessing the array of memory cells.

27. (Previously Presented) The memory device of claim 26, wherein the first plate comprises a single crystalline layer upon which is formed the layer of polysilicon.

28. (Canceled)

29. (Previously Presented) The memory device of claim 26, wherein the second plate comprises polysilicon.

30. (Canceled)

31. (Previously Presented) A memory cell, comprising:

a transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a second source/drain region, a body region and a first source/drain region vertically aligned with the second source/drain region;

a trench capacitor including a first plate coupled to the second source/drain region without an intervening conductor; and

wherein the trench capacitor further includes a polysilicon second plate formed in a trench, the polysilicon second plate surrounding at least a portion of the first plate, the first plate

including a surface layer of polysilicon that is etch-roughened, and an insulator layer that separates the polysilicon second plate from the etch-roughened polysilicon surface of the first plate, wherein the transistor further includes a gate adjacent to the body region and the gate being directly above the polysilicon second plate.

32. (Previously Presented) The memory cell of claim 31, wherein the first plate comprises heavily doped n-type silicon.

33. (Canceled)

34. (Previously Presented) A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the vertical transistor including a first source/drain region, a body region, and a second source/drain region vertically aligned with the first source/drain region and the body region; and

a trench capacitor including a single crystalline silicon first plate coupled to the second source/drain region without an intervening conductor, and a second plate formed in a trench, the first plate including a layer of polysilicon having an etch-roughened surface, the second plate surrounding at least a portion of the etch-roughened surface of the first plate; and

wherein the vertical transistor further includes a gate adjacent to the body region and the gate being directly above the second plate.

35.-36. (Canceled)

37. (Previously Presented) The memory cell of claim 31, wherein the second source/drain region is P-doped or N-doped.

38. (Canceled)

39. (Previously Presented) The memory cell according to claim 34, wherein the single crystalline polysilicon is P-doped or N-doped.

40. (Canceled)

41. (Currently Amended) A memory cell, comprising:

a transistor comprising outwardly from a substrate of a second source/drain region, at least a portion of the second source/drain region serves as a single crystalline first capacitor plate of a trench capacitor for allowing the transistor to couple to the trench capacitor through a second source/drain region and the first capacitor plate without an intervening conductor, the transistor also comprising a body region, and a first source/drain region vertically aligned with the second source/drain region, wherein the first capacitor plate includes a micro-roughened surface for increasing the capacitance of the trench capacitor;

the trench capacitor being formed in a trench surrounding a portion of the transistor and including a second capacitor plate of polycrystalline material formed so as to surround the first capacitor plate; and

an insulator layer that separates the second polycrystalline plate from the micro-roughened surface of the first plate, wherein the transistor further includes a gate adjacent to the body region and the gate being directly above the second plate.

42. (Previously Presented) A memory cell according to claim 41, wherein the micro-roughened surface of the first capacitor plate comprises a layer of polysilicon.

43. (Previously Presented) The memory cell according to claim 41, wherein the second source/drain region that includes the first capacitor plate, the body region, and the first source/drain region are formed as a pillar of single-crystal semiconductor material.

44. (Previously Presented) The memory cell according to claim 41, wherein the second plate also surrounds first plates of adjacent memory cells.

45. (Previously Presented) The memory cell according to claim 44, wherein the second plate is grounded.

46. (Previously Presented) The memory cell according to claim 17, wherein the second plate also surrounds first plates of adjacent memory cells.

47. (Previously Presented) The memory device according to claim 26, wherein the second plate also surrounds first plates of adjacent memory cells.

48. (Previously Presented) The memory cell according to claim 31, wherein the second plate also surrounds first plates of adjacent memory cells.

49.-51. (Canceled)

52. (Currently Amended) A memory cell comprising:

a vertical transistor formed on a substrate, the vertical transistor including a first source/drain region, a body region, and a second source/drain region vertically aligned with the first source/drain region and the body region;

a trench capacitor including a first plate coupled to the second source/drain region without an intervening conductor, and a second plate formed in a trench and surrounding the first plate, the first plate having an etch-roughened surface, the second plate having a top surface; and

a word line for activating the vertical transistor, the word line being formed directly above the top surface of the second plate.

53. (Currently Amended) A memory device comprising:

an array of memory cells, each of the memory cells including a vertical transistor and a trench capacitor, the vertical transistor including a body region, a first source/drain region, and a second source/drain region vertically aligned with the body region and the first source/drain region, the trench capacitor including a first plate coupled to the second source/drain region

without an intervening conductor, and a second plate formed in a trench and surrounding the first plate, the first plate including a micro-roughened surface of polysilicon;

a plurality of word lines for activating the vertical transistor of each of the memory cells, each of the word lines being formed directly above a top surface of the second plate of trench capacitor; and

a plurality of bit lines, each of the bit lines is coupled to a selected [[a]] number of the memory cells at the first source/drain region of the vertical access transistor of each of the selected number of the memory cells.

54. (Previously Presented) The memory cell of claim 52, wherein the first plate comprises heavily doped n-type silicon.

55. (Previously Presented) The memory cell of claim 52, wherein the second source/drain region includes one of P-doped material and N-doped material.

56. (Previously Presented) The memory cell of claim 53, wherein the first plate comprises heavily doped n-type silicon.

57. (Previously Presented) The memory cell of claim 53, wherein the second source/drain region includes one of P-doped material and N-doped material.